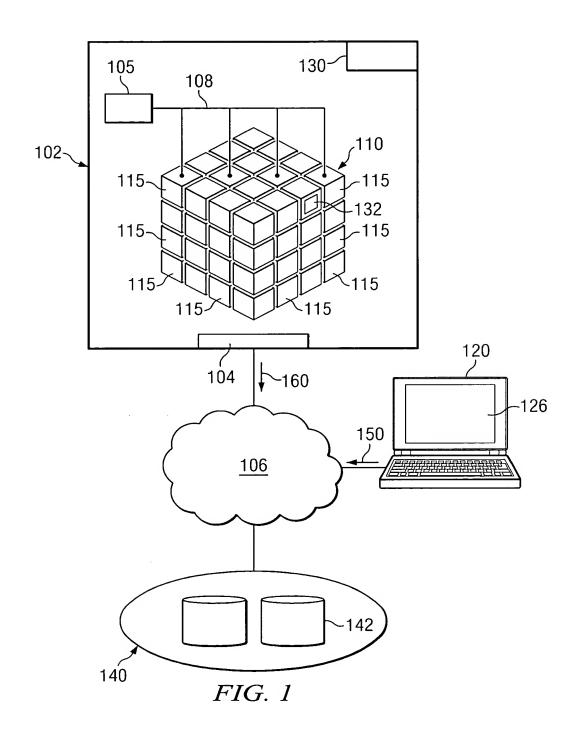
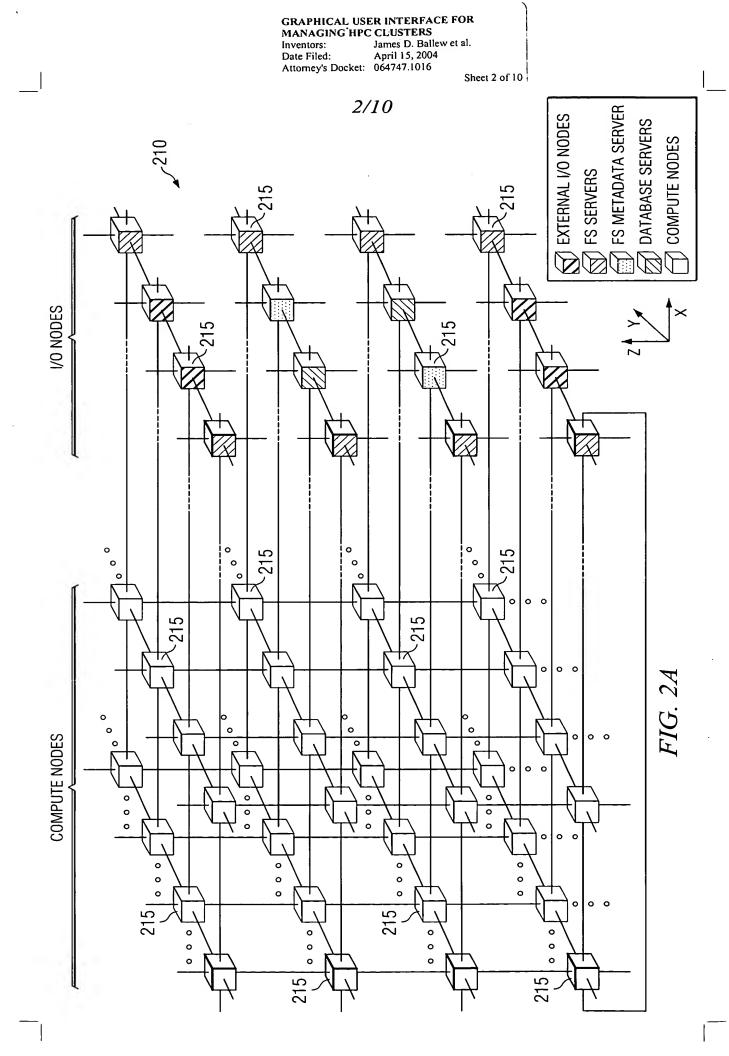
Inventors: James D. Ballew et al.
Date Filed: April 15, 2004
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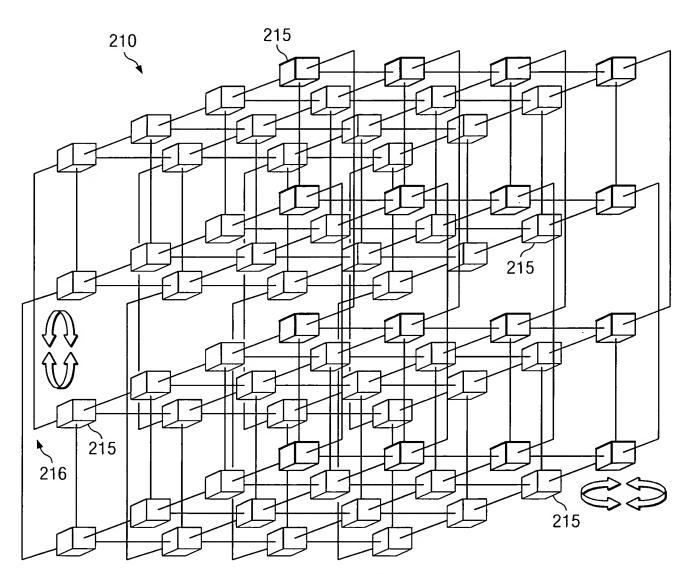
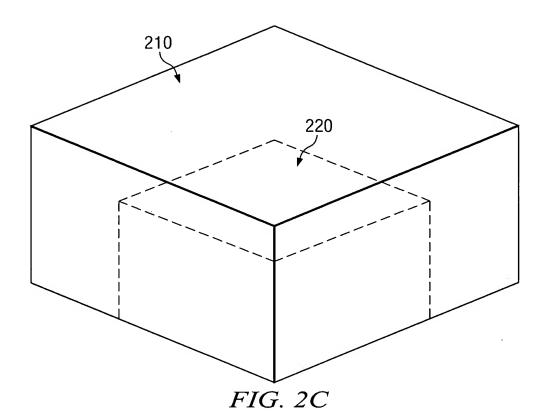


FIG. 2B

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210 220 230b 230a

FIG. 2D

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GB ETHERNET

MANAGEMENT INFRASTRUCTURE

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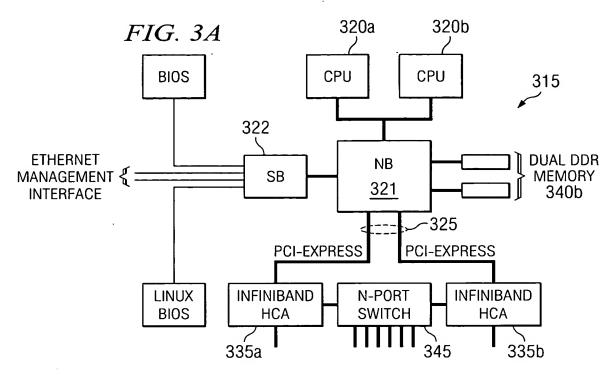


FIG. 3B MOTHERBOARD WITH PCI EXPRESS **HYPER HYPER** 320a 320b **TRANSPORT** TRANSPORT **HYPER** DUAL DDR **DUAL DDR** TRANSPORT **CPU MEMORY MEMORY** CPU 340a 340b 325 HYPER **HYPER TRANSPORT TRANSPORT** HT/PCI HT/PCI ·330b 330a-**BRIDGE BRIDGE PCI-EXPRESS PCI-EXPRESS HCA HCA** 335b 335a-345

N-PORT SWITCH

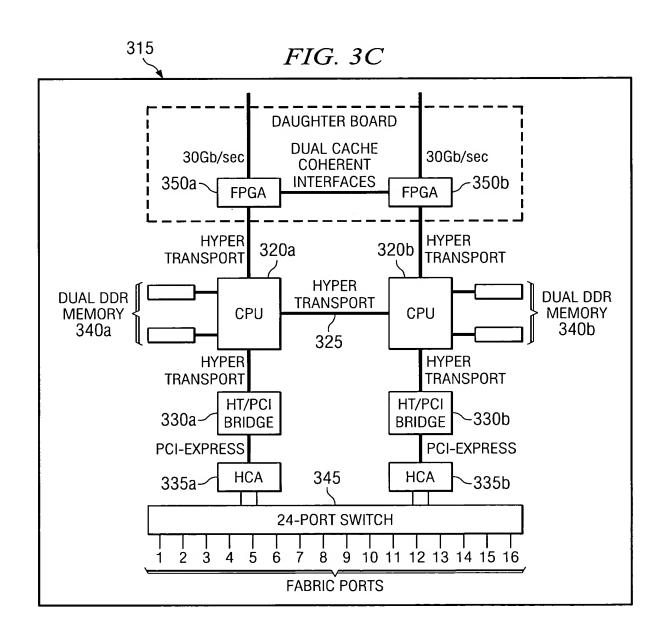
GB ETHERNET MANAGEMENT

INFRASTRUCTURE

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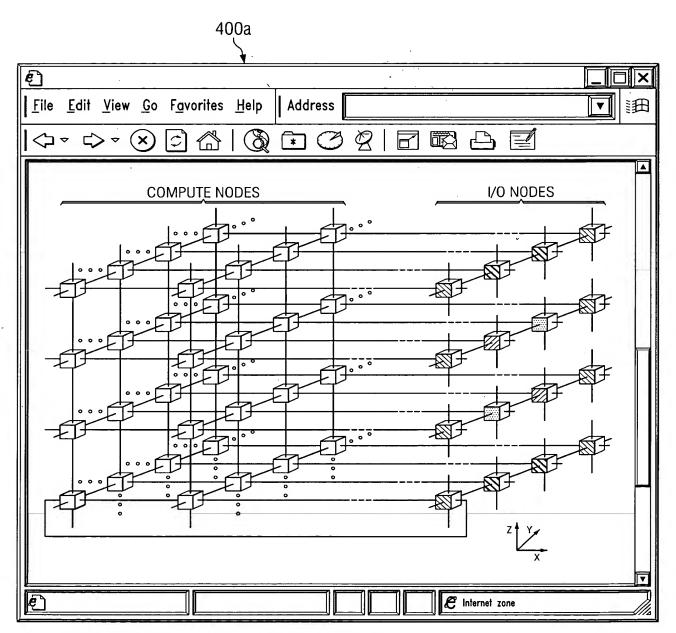
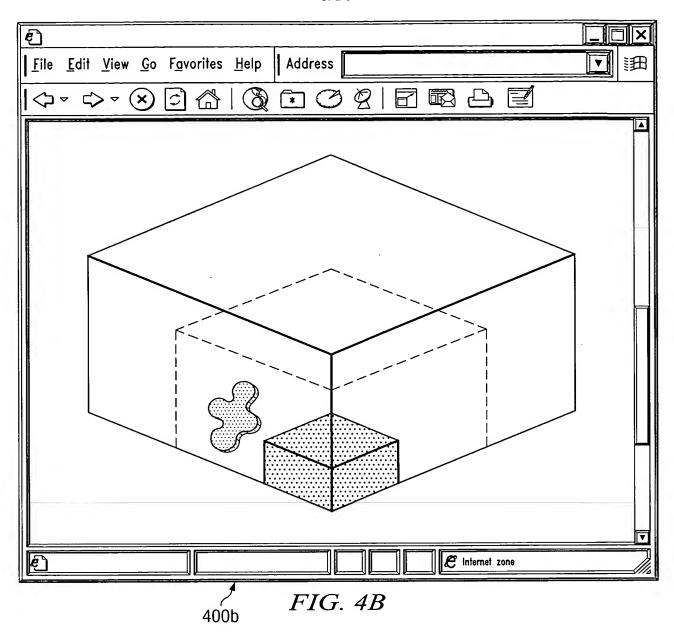
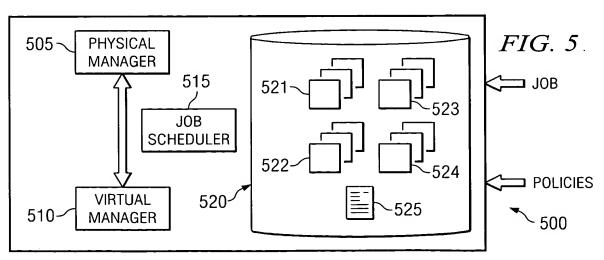


FIG. 4A

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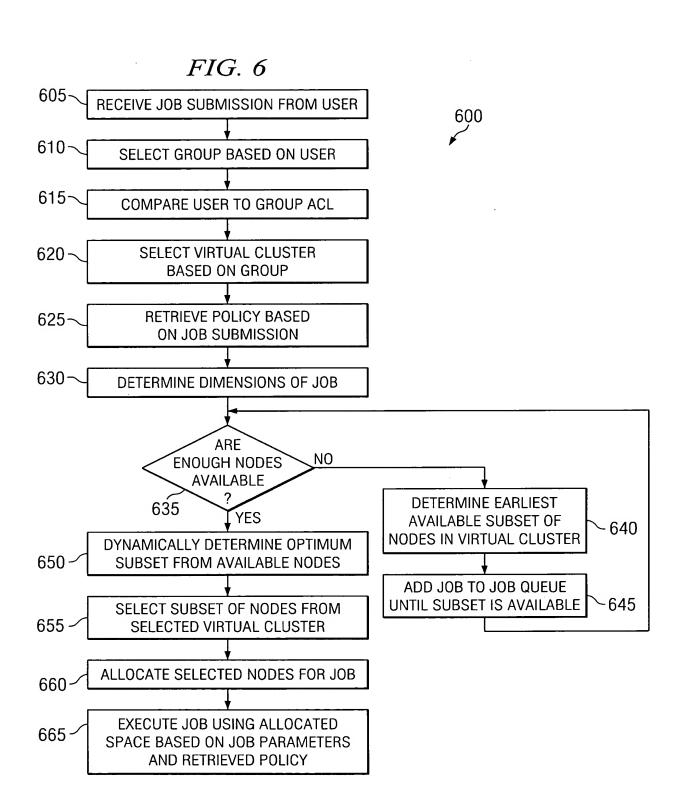




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